REMARKS

The above amendment is made in response to the Office action of October 26, 2005. The Examiner's reconsideration is respectfully requested in view of the above amendment and the following remarks.

Claims 1, 8 and 12 have been amended. Claims 1-14 are pending in the present application. Applicant gratefully acknowledges the Examiner's indication of the allowability of claims 8-10, but for their dependence on rejected base claims. No new matter has been added.

Claim Objections

Claims 1-14 stand objected to because the Examiner alleges that acronyms such as "SRAM" and "DRAM" should not be used to abbreviate key terms or phrases until they are explicitly defined previously within the claim, or in a claim to which it depends. Further, the Examiner points out that recitation of "DRAM calls" in claim 8 should be -- DRAM cells --. Claims 1, 8 and 12 have been amended to reflect the corrections suggested by the Examiner.

Therefore, it is respectfully requested that the objection to claims 1-14 be withdrawn.

Claim Rejections – 102(b)

Claims 12 and 14 –16 stand rejected under 35 U.S.C. § 102 (b) as being anticipated by Leung et al. (U.S. Patent No. 5,999,474) for the reasons stated on pages 3-5 of the Office action. Applicants respectfully traverse.

To anticipate a claim under 35 U.S.C. § 102, a single source must contain all of the elements of the claim. *Lewmar Marine Inc. v. Barient, Inc.*, 827 F.2d 744, 747, 3 U.S.P.Q.2d 1766, 1768 (Fed. Cir. 1987), *cert. denied*, 484 U.S. 1007 (1988). Moreover, the single source must disclose all of the claimed elements "arranged as in the claim." *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 716, 223 U.S.P.Q. 1264, 1271 (Fed. Cir. 1984).

It is respectfully submitted that Leung requires an additional element of a SRAM cache such that all write data is initially written to the SRAM cache before being written

to the memory banks, and all read data provided to the external data bus is stored in the SRAM cache. (Col. 2, lines 43-58.) In particular, Leung requires a SRAM cache in preparation of an overlap of the refresh operation. Thus, the structure and operation disclosed by Leung are more complicated compared to the present application.

In contrast, each memory bank of the present application saves data up to one (1) bit, and therefore, in order to operate properly, eight (8) memory banks are needed (e.g., for an eight-bit byte). Each memory bank performs read, write and refresh operations independently. Conversely, each memory bank of Leung saves eight bits, therefore, during normal operation, only one memory bank operates.

The Examiner states that the present invention determines "whether a refresh operation or a write operation for a previous frame is being performed in the memory banks." However, Leung merely teaches the relation between the refresh and write operations, and does not teach or suggest delaying a write operation in the previous frame. Leung discloses that the read and write operations always have priority over the refresh operation, and as a consequence, there is no decrease in speed since the refresh operation starts only after the read/write operations are complete. Thus, Leung does not address the problem of delayed write operation during the refreshing process.

Leung et al. do not teach or suggest, providing multiple pieces of input data to the memory banks, **each piece of the input data corresponding to a single bit being provided separately to corresponding one of the memory banks; determining whether a refresh operation or a write operation for a previous frame is being performed in the memory banks; storing a piece of the input data in a data buffer if the refresh operation or the write operation is being performed in a certain memory bank for both the refresh and write operations, wherein the piece of the input data is provided to the certain memory bank *and write operation of the piece of the input data is suspended***; and writing the piece of the input data stored in the data buffer into DRAM cells of the certain memory bank after the refresh operation or the write operation is completed; wherein the memory banks except for the certain memory bank independently perform write operations, while the refresh operation or the write operation for the previous frame is performed with respect to the certain memory bank,

as in amended claim 12. Thus, claim 12, including claims depending therefrom, i.e., claims 13 and 14, define over Leung et al.

Accordingly, Applicants respectively request that the rejections to claims 12 and 14 be withdrawn.

Claim Rejections – 103(a)

Claims 1, 2, 5, 6 and 11 stand rejected under 35 U.S.C. § 103 (a) as being unpatentable over Leung et al. in view of Fujioka et al. (U.S. Patent Application Publication No. 2003/0106010) for the reasons stated on pages 5- 9 of the Office action. Applicants respectfully traverse.

As discussed above with respect to Leung above, Fujioka also fails to teach or suggest how to address the problem of delayed write operation during the refreshing process. Further, both Leung and Fujioka are silent with respect to the parity bank in the refresh operation and in the delayed write operation. Conversely, the instant application defines the two.

When a memory bank of the present application is refreshing, the read operation can be omitted and the respective bits can be compensated as parity. However, the write operation cannot be omitted when the memory bank is refreshing, and thus, the data has to be recorded in the respective bank after the refreshing process. The BCON0 – BCON7 and BCONP signals, described with reference to FIG. 5 of the present application, are used to determine the banks that are not able to perform the read/write operations.

In Leung, the SRAM cache must be included, and thus Leung is structurally different from the present application. In Fujioka, the parity bank and data bank each comprises of DRAM cells, and therefore, the refresh operation for the data bank and parity bank must be considered in order to operate properly. Also, in order to operate properly, the refresh operation (REF Section) and the delayed write operation (IWR1 – IWR6) as in FIG. 5 of the present application must be considered. However, neither Leung nor Fujioka, taken alone or in combination, addresses the problem of delayed write operation during the refreshing process, whereas the present application solves the problems that arise during the read and write operations.

Neither Leung et al. nor Fujioka et al., teach or suggest, either alone or in combination, the plurality of **memory banks configured to separately store input data corresponding to a single bit in DRAM cells** specified by an input address externally provided, **wherein write operations of the memory banks are independently controlled such that when a refresh operation or a write operation for a previous frame is being performed in a certain memory bank, write operation of input data is independently performed with respect to the respective memory banks except for the certain memory bank in both of the refresh and write operations**; a parity generator for generating an input parity based on the input data, the input parity having a certain preset parity value in conjunction with the input data; and a parity bank for storing the input parity, as in amended claim 1. Thus, claim 1, including claims depending therefrom, i.e., claims 2-12, define over Leung et al. in view of Fujioka et al.

Accordingly, Applicants respectively request that the rejections to claims 1, 2, 5, 6 and 11 be withdrawn.

Claims 3 and 4 stand rejected under 35 U.S.C. § 103 (a) as being unpatentable over the combined teachings Leung et al. and Fujioka et al. in view of MacLaren et al. (U.S. Patent Application Publication No. 2002/0016942) for the reasons stated on pages 9 and 10 of the Office action. Applicants respectfully traverse.

It is respectfully pointed out that claims 3 and 4 depend from claim 1, which is submitted as being allowable for defining over Leung and Fujioka either alone or in combination as discussed above. Furthermore, it is respectfully submitted that use of the of the error detection system allegedly taught in MacLaren does not cure the deficiencies noted above with respect to Leung and MacLaren either alone or in combination.

Accordingly, Applicants respectively request that the rejections to claims 3 and 4 be withdrawn.

Claim 7 stands rejected under 35 U.S.C. § 103 (a) as being unpatentable over the combined teachings Leung et al. and Fujioka et al., and in further view of Tsukude (U.S.

Patent Application Publication No. 2003/0185078) for the reasons stated on pages 11 and 12 of the Office action. Applicants respectfully traverse.

It is respectfully pointed out that claim 7 depends from claim 1, which is submitted as being allowable for defining over Leung and Fujioka either alone or in combination as discussed above. Furthermore, it is respectfully submitted that use of the of the flag generator for generating a refresh flag signal tot eh control allegedly taught in Tsukude does not cure the deficiencies noted above with respect to Leung and MacLaren either alone or in combination.

Accordingly, Applicants respectively request that the rejections to claim 7 be withdrawn.

Conclusion

In light of the above amendment and remarks, the present application, including claims 1-14, is believed to be in condition for allowance.

Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the outstanding rejections. If there are any charges due with respect to this response, please charge them to Deposit Account No. 06-1130 maintained by Applicant's Attorneys.

Respectfully submitted,

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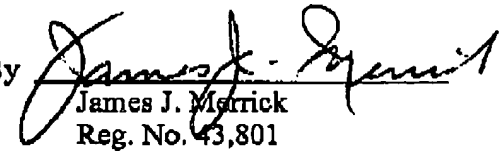
By 

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Date: January 26, 2006